A Tunable Dual-Edge Time-to-Digital Converter

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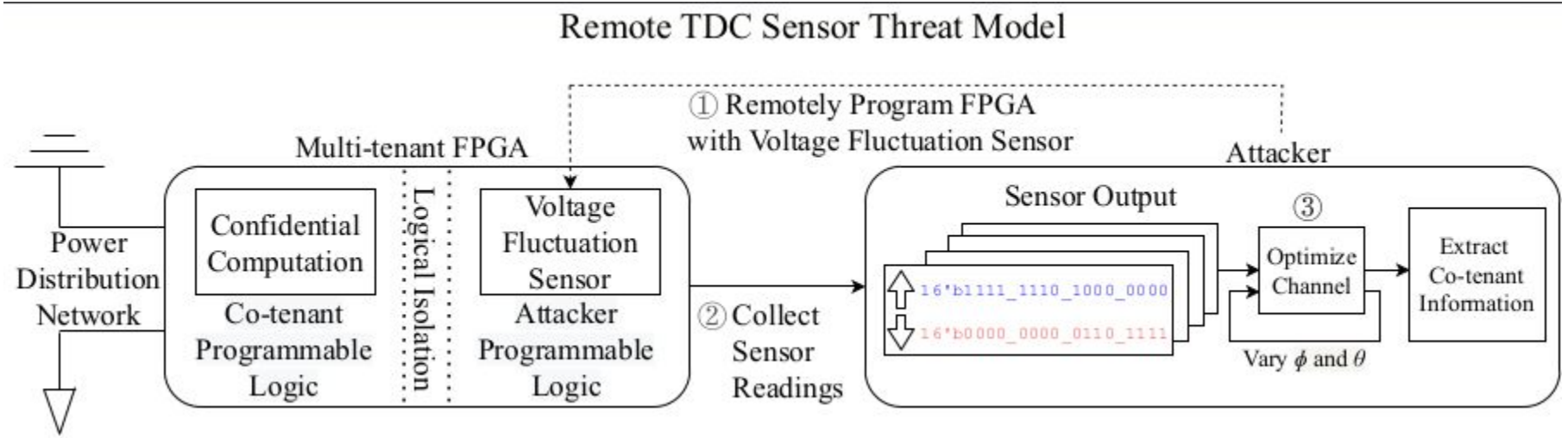
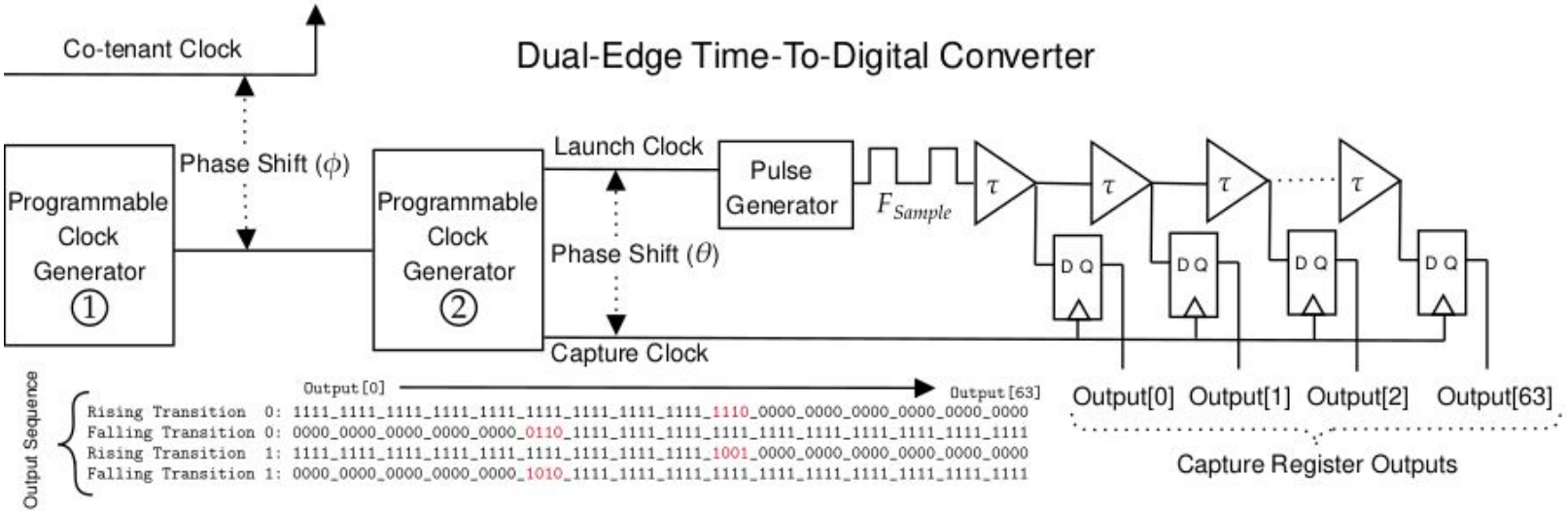
Threat-Model

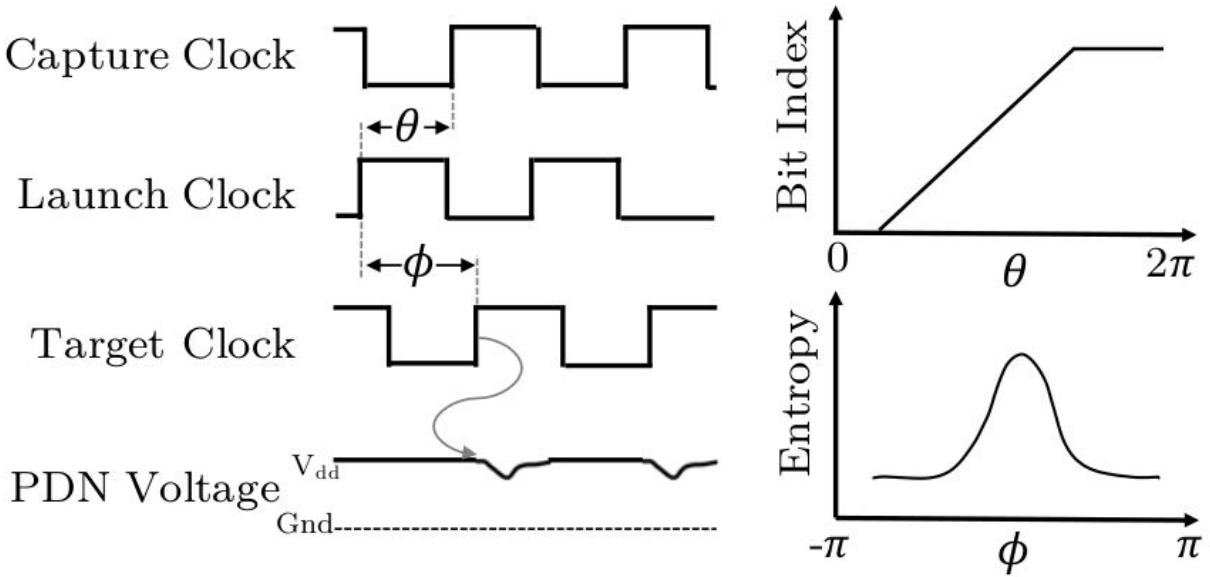


Time-to-Digital Converters

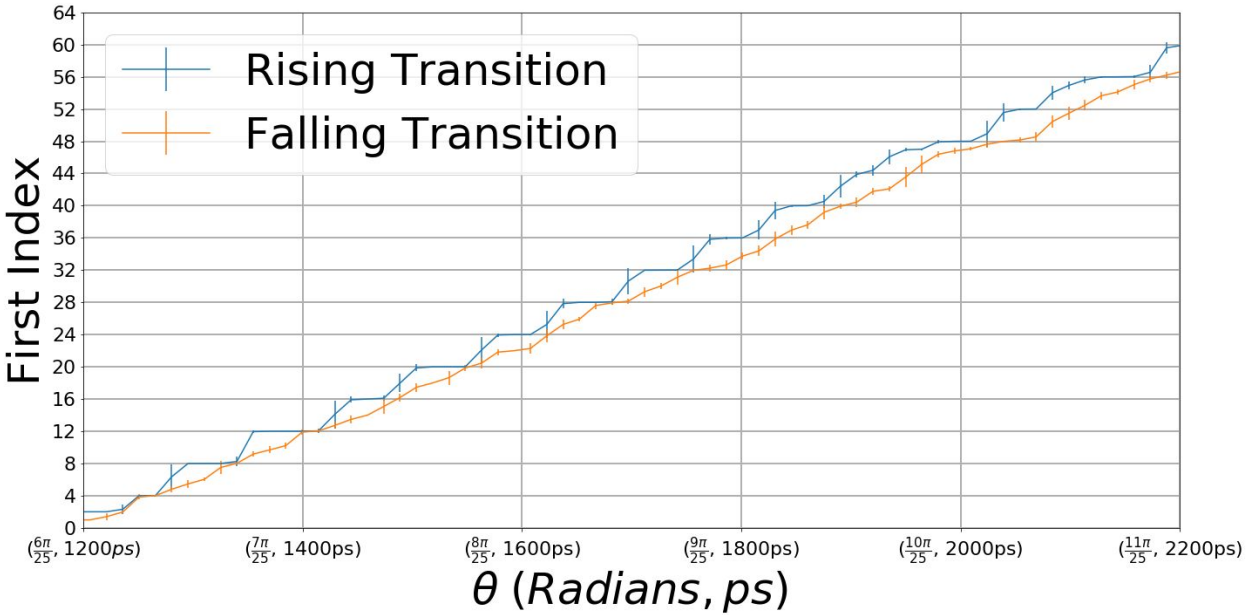
Measure propagation delay of a rising and falling transition through an array of logic elements



How can we improve signal resolution?

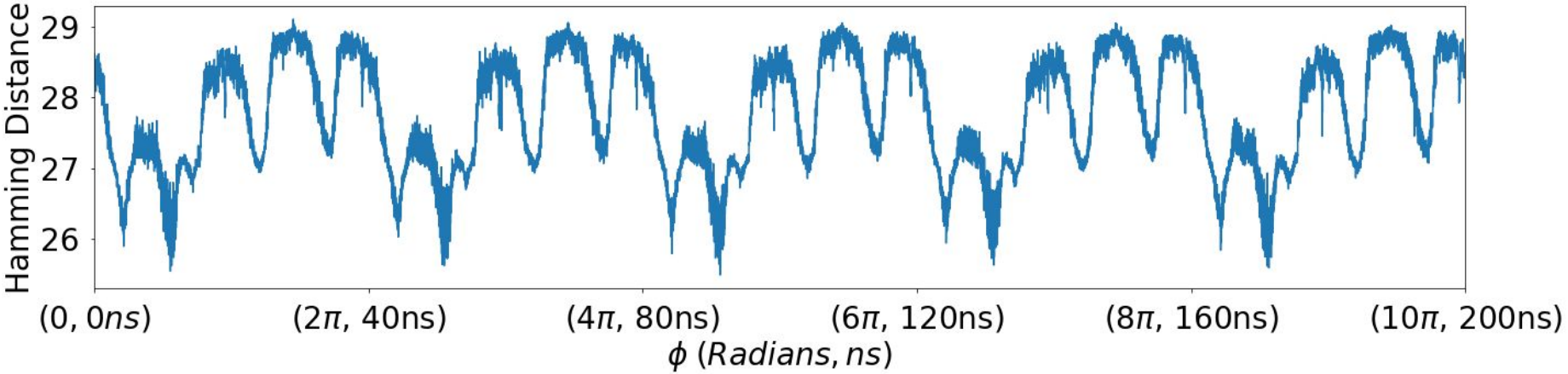


Capture/Launch Clock Delay Tuning (θ)

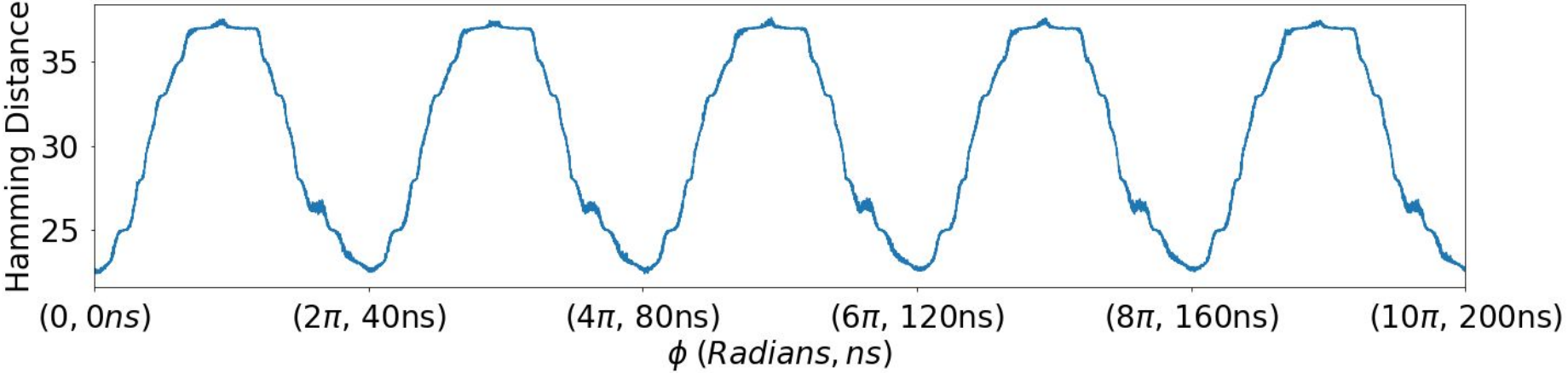


Target Clock Tuning (Φ)

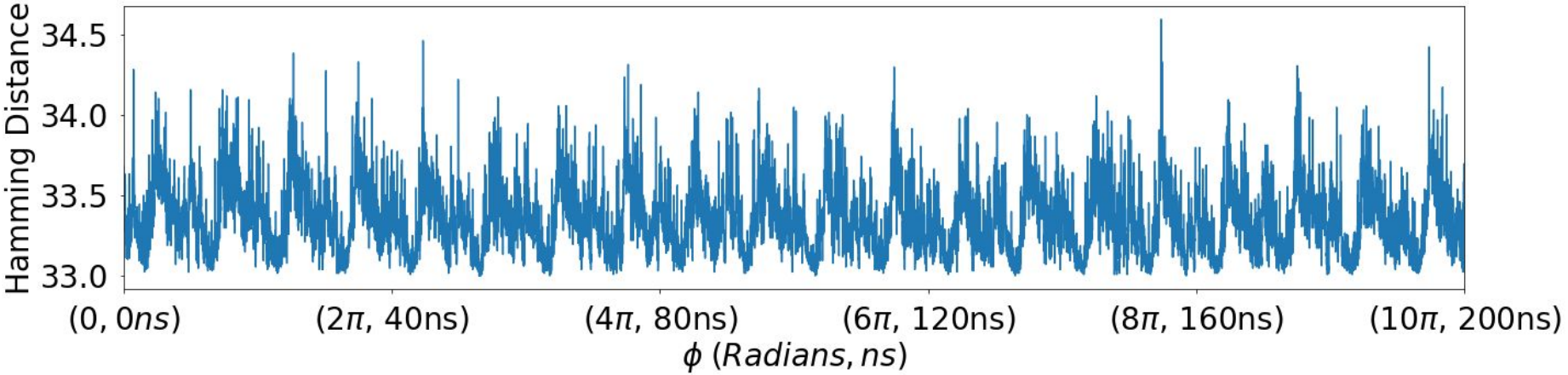
Orca Soft-Processor running AES



25MHz Power-Wasters



Baseline (no co-tenant)



A Classification Test

We instantiate nine “co-tenant” applications alongside the Tunable Dual-Edge Time-to-Digital Converter

Three soft-processors running AES and PRESENT cipher (6 total)

“Baseline,” or the absence of a co-tenant

Combinatorial power-wasters

AES running as an HLS core

Leveraging These Tools

Dataset 1:

1. Tune launch-capture delay (θ) to point of greatest linearity
2. Tune target phase relationship (Φ) to point of highest falling transition variance

Dataset 2:

3. Tune launch-capture delay (θ) to point of greatest linearity
4. Tune target phase relationship (Φ) to point of minimum falling transition variance

Max-tuned

Min-tuned